Demonstration of a Sub-Millimeter Wave Integrated Circuit (S-MMIC) using InP HEMT with a 35-nm Gate

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***Abstract*— In this paper, we present two single stage MMIC amplifiers with the first demonstrating a measured S21 gain of 3-dB at 280-GHz and the second demonstrating 2.5-dB gain at 300-GHz, which is the threshold of the sub-millimeter wave regime. The high-frequency operation is enabled by a high-speed InP HEMT with a 35-nm gate. This is the first demonstrated S21 gain at sub-millimeter wave frequencies in a MMIC.**

***Index Terms* — Low Noise Amplifier, HEMT, MMIC, S-MMIC, Millimeter-Wave, Sub-millimeter wave, Coplanar Waveguide**

I. Introduction

The sub-millimeter wave regime begins at frequencies above 300-GHz where wavelengths are less than 1-mm. Traditionally, receiver applications at short mm-wave frequencies to sub-millimeter wave frequencies, such as atmospheric sensing and radio-astronomy, have relied on mixer front-ends [1] and sophisticated technologies have been developed to support this [2]. However, developing low-noise active electronics at these frequencies would lead to significant improvements in receiver sensitivity. In this paper we report MMIC results at the sub-millimeter wave threshold, including a 280-GHz single stage amplifier using a common-source device and a 300-GHz single stage amplifier using a common-gate device, both of which use an InP HEMT with a new 35-nm gate process. A SEM of a 35-nm gate from a gate development lot is shown in Figure 1. These simple single stage MMICs shows low-noise active electronics to be a viable technology to sub-millimeter wave frequencies. In particular, both single-stage amplifiers demonstrate measured S21 gain to frequencies above 300-GHz. To our knowledge, this is the first measured transistor gain at sub-millimeter wave frequencies. For this reason, we refer to the circuits in this paper as S-MMICs, where the "S" denotes sub-millimeter wave operation.

Recently, significant progress has been made in pushing HEMT MMIC amplifiers towards the sub-millimeter wave threshold, including a 4-stage MMIC amplifier using 50-nm MHEMT in [3] which demonstrated 15-dB gain at 220-GHz and a 3-stage microstrip MMIC amplifier using a 70-nm gate HEMT which demonstrated 10-dB at 235-GHz [4].

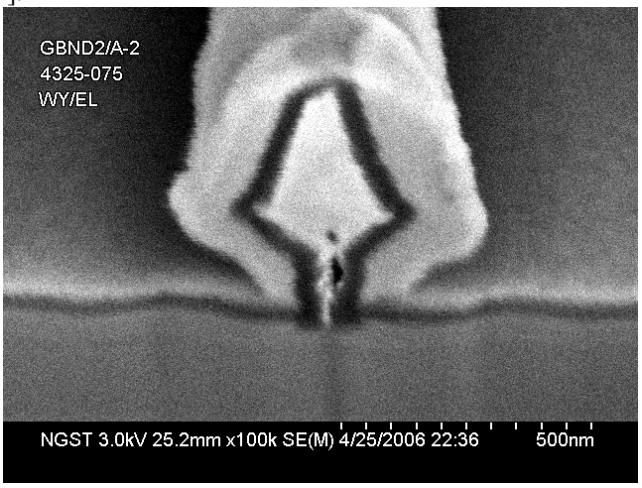

Figure 1 SEM cross-Section of 35-nm gate used in this work.

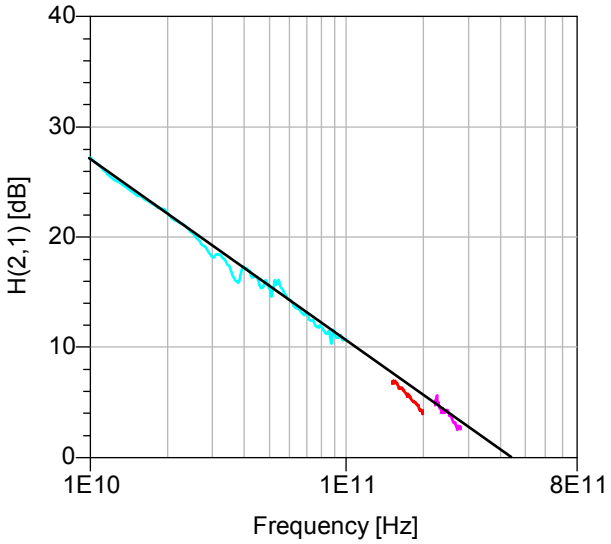

Figure 2 H21 of a 2-finger 35-nm HEMT device with 30-µm total periphery de-embedded to device reference plane. Note that the three measurements are "stitched together" to look at broadband device performance. A straight line fit of data from 10-280 GHz gives an estimate of f_T above 400-GHz.

In this paper we present the first MMIC amplifier results of a 35-nm HEMT process. Additionally, we have performed multi-band device measurements on a two finger device with

a total periphery of 30-µm. A plot of H(2,1) is shown in Figure 2. Note that the blue trace is measured at Northrop Grumman Corporation on an XF VNA probe station from 0.05-110-GHz, and the red and magenta traces are measured at the Jet Propulsion Laboratory (JPL) on a WR-5 and WR-3 based probe station. The high and low frequency data were by necessity taken on different sites due to required probe layouts and then de-embedded to the same reference plane. From Figure 2, a simple straight-line fit of H(2,1) gives an f_T >400-GHz.

II. Development of 35-nm InP HEMT Transistor

The InP HEMT epi wafers used in this work were grown by MBE. The structure employs psudomorphic InGaAs channel with 75% indium and a silicon delta-doping layer as the electron supply layer. Room temperature electron mobility over 12000 cm2/V.s is achieved with a sheet charge of 3.5e12 cm-2. The Ohmic contact is formed with a Ge/Ni/Au metal and results in a low contact resistance of 0.11 Ohm.mm. Ti/Pt/Au was used as the gate metal to form a reliable Schottky contact. Excellent DC performance was achieved on these devices, including a peak Gm as high as 1.6 S/mm and a breakdown voltage over 2.5V, which is needed for power applications. The measured DC-IV for a device with 35-nm gate is shown in Figure 4.

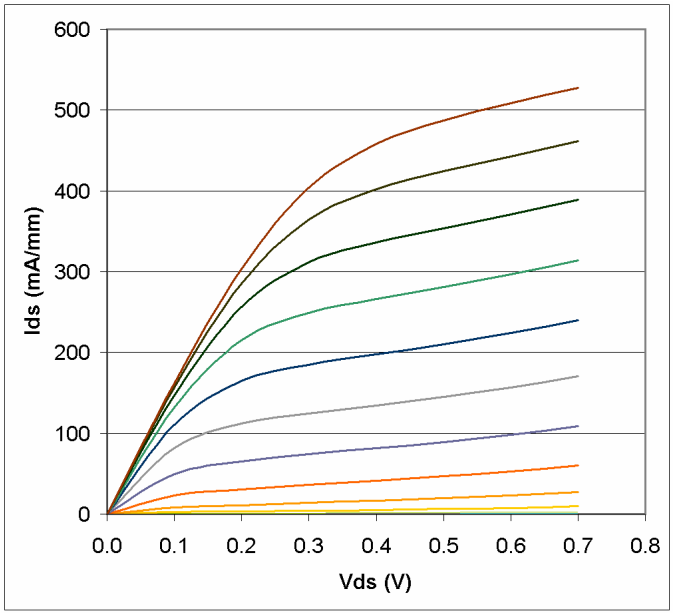

Figure 3 Plot of DC-IV curves for 35-nm HEMT device.

A key approach in this process is the 35nm gate formed with our proprietary e-beam lithography. A bilayer PMMA/copolymer MMA resist strategy was used to create repeatable, high resolution, self-aligned t-gate openings. E-beam lithography was performed using a Leica EBPG5000 operating at 20keV and 50keV. A cross-section of the gate is shown in the SEM picture of Figure 1. From our measurements, Cgs is successfully reduced by 50% from our 70nm devices which was used to obtain the results in [4], and should be capable of achieving considerable higher operating frequencies.

III. Circuit Design and Measurement Results

In addition to device evaluation structures, our first dedicated 35-nm mask contains simple single-stage amplifiers. To aid in the design of the single-stage amplifier, we have developed a device model extrapolated from the 70-nm InP HEMT process used for the results in [4]. Most of the extrapolated parameters consist of simple "guesses" on capacitance scaling and resistance scaling based on the device layout and desired gate profile. The model inductances are purely based on EM simulations of the device feeds. At this time we are working on using our measured device and single-stage amplifier data to build a more accurate model based on measurements.

Using the original estimated model, we developed a set of common-source and common-gate single stage amplifiers at a variety of frequencies and device sizes. The amplifiers themselves are implemented in coplanar waveguide (CPW). So that measured vs. modeled as simple as possible for model development and verification, the DC is injected through the gate and drain probes. Thin Film Resistors (TFR) are used on the common-gate single-stage amplifiers to improve stability, but are not included in the common-source circuits. This also helps in de-embedding the device performance since losses will be minimized thereby keeping the dynamic range of the measurement as good as possible. A microphotograph of one of the common-source amplifiers is shown in Figure 4. From the original extrapolated model, this single-stage amplifier was designed to have a center frequency of 300-GHz. Although the pads for backside vias are clearly visible, all of the results that we have taken to date are on unthinned InP substrates (25-Mil) with no backside processing. Our first wafers are currently going through backside processing and we will re-evaluate performance after they are processed.

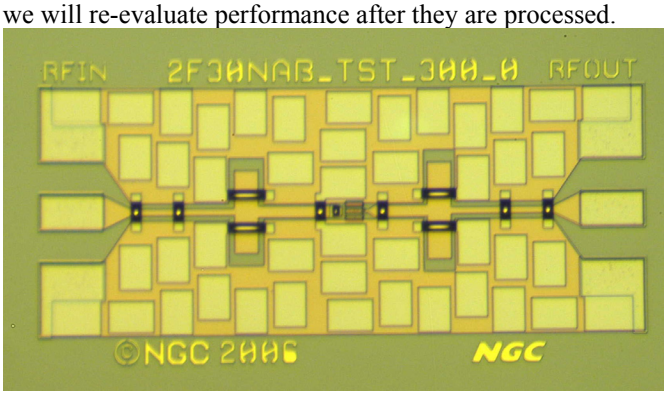

Figure 4 Microphotograph of a single-stage common source amplifier optimized for a 300-GHz center frequency.

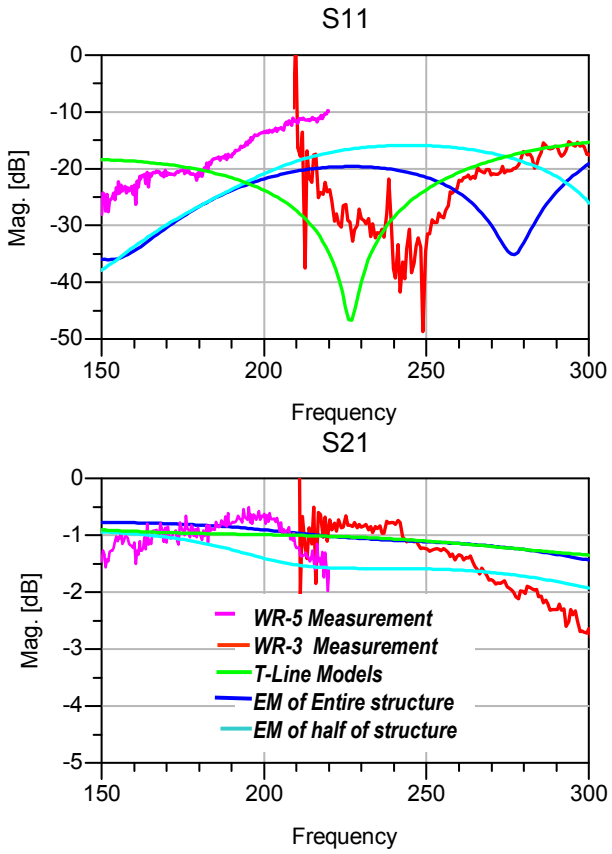

Figure 5 Measured and Modeled MAG and K-factor for 2-finger, 80-um device biased at 0.15-V and 40-mA/mm. Note that the red trace is modeled.

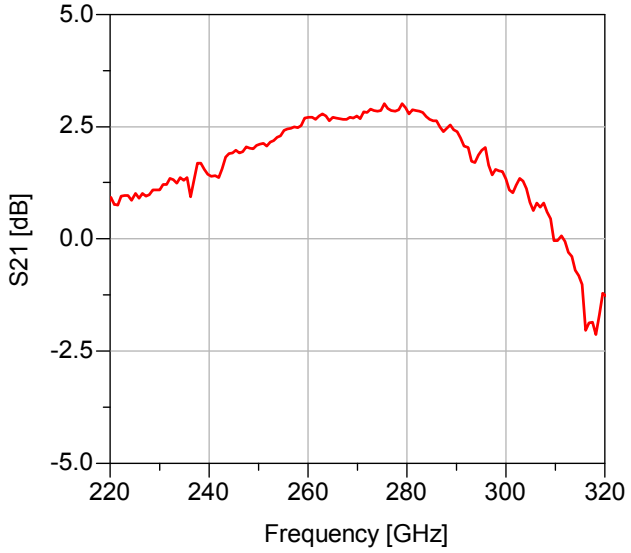

Figure 6 Measured results for a single-stage common source amplifier designed for a center frequency of 300-GHz using two finger devices with a total device periphery of 30-µm.

Since this is our first experience with this process, we have designed the test structures to be probeable at a variety of frequency bands. To do this, a variety of probe pitches are used for the test structures, including a launch layout compatible with both 100-µm pitch for lower frequency measurements (<110-GHz) and 80-µm pitch for WR-5 based probes from GGB for measurements up to 200-GHz, and a launch for 60-µm pitch for WR-3 based probes from GGB for measurements up to 325-GHz. We have also included structures with a 50-µm launch for WR-2.2 based probes. Note that the WR-5 probes can also fit on the WR-3 launch if required. Although WR-2.2 based frequency extenders are commercially available, to date no WR-2.2 based probes have been developed. However, including the 50-µm pitch launches will allow us to perform higher frequency characterization if they are developed in the future. All measurements have been taken with using probetip calibration.

A through measurement using a probe-tip calibration is shown in Figure 5 for the same structure measured with both the WR-5 and WR-3 probes. The other traces on the plot are simple CPW transmission line simulation of the structure (green), an electromagnetic simulation of the entire structure using Momentum software (dark blue) and the cascaded electromagnetic simulation of the bisected half of the structure (light blue). For the EM simulation, the thick metal features of the Momentum simulator were enabled and a fine meshed was used of 50-cells per wavelength at 350-GHz with 6-cells across for the transmission lines. Momentum is used because the unthinned InP substrate may have appreciable amounts of substrate modes that should be modeled with an open-box solver.

Although there is a fair amount of disagreement between measurement and the various simulations, this does illustrate the difficulty of doing precise on-wafer measurements at these extreme frequencies. In particular, measured S21 drops off quickly after 250-GHz. This may be due to a variety of sources, including substrate coupling, radiation, or capacitive effects to probe-placement precision not perfectly calibrated out. This would be due to capacitive loading effects of the probe launch if the probes land further inside the launch during the through line measurement than during the calibration.

Measured results for a single stage common-source amplifier using two finger devices with a total periphery of 30-µm is shown in Figure 6. The circuit was designed for a center frequency of 300-GHz. This is the circuit shown in Figure 4. In the measurement, the center frequency shifted to 280-GHz

Measured peak gain was 3-dB with the probe tip calibration. No attempt was made to offset the losses of the launch, which may be fairly significant based on the through line data shown in Figure 5. Further, we expect that the gain may modestly improve after backside processing due to the reduction of energy coupled to substrate modes. Additionally, 1.25-dB gain is measured at 300-GHz, the threshold of the sub-millimeter wave regime.

We have also obtained measurement results on common-gate single-stage amplifiers. Common-gate stages are necessary in cascode type designs that have demonstrated excellent mm-wave performance [3]. For this reason, we have also included single-stage common-gate amplifiers at various frequencies with several device sizes. Common-gate amplifiers are typically difficult to stabilize at high frequencies due to series inductance between the device gate and ground. For this reason, we have included a shunt TFR network at the gate for low frequency stability and a series 10-ohm resistor at the drain. Measured results of a circuit using two finger devices with a total of 20-µm of periphery. The amplifier is designed for a center frequency of 270-GHz. Measured performance is shown in Figure 7. Peak gain of 2.5-dB is measured centered at 300-GHz. Again, no attempt has been made to de-embed the losses of the launch which may be appreciable at these frequencies. Additionally, this circuit does have TFR resistors which reduces gain as well as enhances stability.

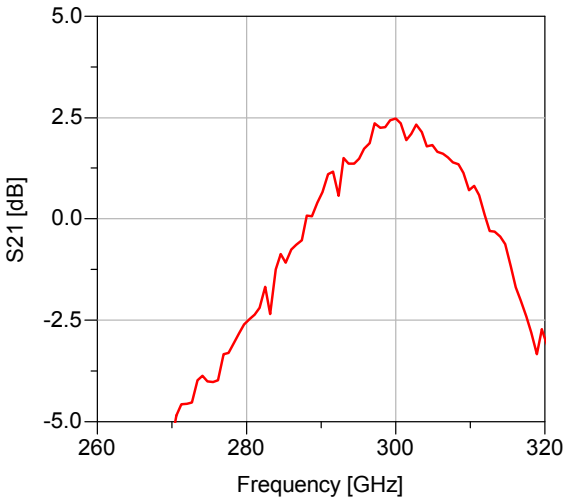

Figure 7 Measured results for a single-stage common gate amplifier designed for a center frequency of 300-GHz using two finger devices with a total device periphery of 20-µm.

IV. Conclusion

In this paper, we present two single stage amplifiers that demonstrate measured S21 gain at frequencies >300-GHz, which is the sub-millimeter wave threshold. For this reason, we refer to these circuits as "S-MMICs". This is the first demonstration of circuit gain at sub-millimeter wave frequencies. The first amplifier uses a common-source device that achieves a measured gain of 3-dB at 280-GHz. The second uses a common-gate device that achieves 2.5-dB gain at 300-GHz. Both of these amplifiers are realized in coplanar waveguide with the results presented here on unthinned substrates.

These results are enabled by a new InP HEMT process which utilizes 35-nm gates. This significantly reduces capacitances and pushes the device f_T to >400-GHz. Based on our initial single-stage results, we expect these devices to enable capable multi-stage low noise amplifiers to frequencies >300-GHz.

Acknowledgement

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